

INVESTOR IN PEOPLE

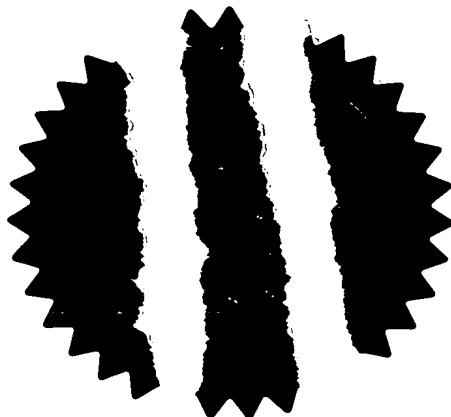
The Patent Office  
Concept House  
Cardiff Road  
Newport  
South Wales  
NP10 8QQ

I, the undersigned, being an officer duly authorised in accordance with Section 74(1) and (4) of the Deregulation & Contracting Out Act 1994, to sign and issue certificates on behalf of the Comptroller-General, hereby certify that annexed hereto is a true copy of the documents as originally filed in connection with the patent application identified therein.

In accordance with the Patents (Companies Re-registration) Rules 1982, if a company named in this certificate and any accompanying documents has re-registered under the Companies Act 1980 with the same name as that with which it was registered immediately before re-registration save for the substitution as, or inclusion as, the last part of the name of the words "public limited company" or their equivalents in Welsh, references to the name of the company in this certificate and any accompanying documents shall be treated as references to the name with which it is so re-registered.

In accordance with the rules, the words "public limited company" may be replaced by p.l.c., plc, P.L.C. or PLC.

Re-registration under the Companies Act does not constitute a new legal entity but merely subjects the company to certain additional company law rules.

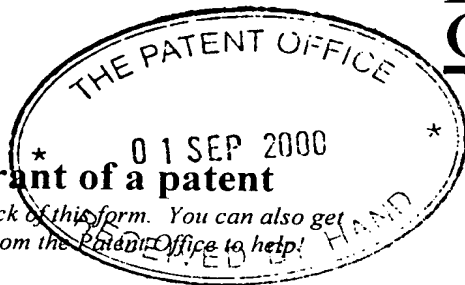


Signed 

Dated 24 SEP 2001



**THIS PAGE BLANK (USPTO)**



# Request for grant of a patent

(See the notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

1. Your reference 102145/VRD/JJH/ms

**31 SEP 2000**

2. Patent application number  
(The Patent Office will fill in this part)

**0021541.8**

3. Full name, address and postcode of the or of each applicant (underline all surnames)

STMicroelectronics Limited  
1000 Aztec West  
Almondsbury  
Bristol  
Avon BS32 4SQ

Patents ADP number (if you know it)

04SEP00 E565295-6 000068  
P01/7700 0.00-0021541.8

If the applicant is a corporate body, give the country/state of its incorporation

United Kingdom

7460272 001

4. Title of the invention

Oscillator

5. Name of your agent (if you have one)

Page White & Farrer

"Address for service" in the United Kingdom to which all correspondence should be sent (including the postcode)

54 Doughty Street  
London WC1N 2LS  
United Kingdom

Patents ADP number (if you know it)

1255003

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and (if you know it) the or each application number

Country

Priority application number  
(if you know it)

Date of filing  
(day / month / year)

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application

Date of filing  
(day / month / year)

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? (Answer 'Yes' if:

Yes

- a) any applicant named in part 3 is not an inventor, or
  - b) there is an inventor who is not named as an applicant, or
  - c) any named applicant is a corporate body
- See note (d))

**Patents Form 1/77**

9. Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document

Continuation sheets of this form -

Description 10

Claim(s) 2

Abstract

Drawing(s) 2 + 1

10. If you are also filing any of the following, state how many against each item.

Priority documents -

Translations of priority documents -

Statement of inventorship and right to grant of a patent (Patents Form 7/77) -

Request for preliminary examination and search (Patents Form 9/77) -

Request for substantive examination (Patents Form 10/77) -

Any other documents  
(please specify)

11. I/We request the grant of a patent on the basis of this application.

Signature

Date

PAGE WHITE & FARRER

01.09.00

12. Name and daytime telephone number of person to contact in the United Kingdom

JUSTIN HILL - 020 7831 7929

**Warning**

*After an application for a patent has been filed, the Comptroller of the Patent Office will consider whether publication or communication of the invention should be prohibited or restricted under Section 22 of the Patents Act 1977. You will be informed if it is necessary to prohibit or restrict your invention in this way. Furthermore, if you live in the United Kingdom, Section 23 of the Patents Act 1977 stops you from applying for a patent abroad without first getting written permission from the Patent Office unless an application has been filed at least 6 weeks beforehand in the United Kingdom for a patent for the same invention and either no direction prohibiting publication or communication has been given, or any such direction has been revoked.*

**Notes**

- a) If you need help to fill in this form or you have any questions, please contact the Patent Office on 0645 500505.
- b) Write your answers in capital letters using black ink or you may type them.
- c) If there is not enough space for all the relevant details on any part of this form, please continue on a separate sheet of paper and write "see continuation sheet" in the relevant part(s). Any continuation sheet should be attached to this form.
- d) If you have answered 'Yes' Patents Form 7/77 will need to be filed.
- e) Once you have filled in the form you must remember to sign and date it.
- f) For details of the fee and ways to pay please contact the Patent Office.

## OSCILLATOR

This invention relates to oscillator circuits and particularly to temperature compensated oscillator circuits.

A problem with many known types of oscillator circuit is that variations in temperature cause changes in the oscillation frequency. In some cases the oscillation frequency can increase with temperature, whereas in other cases the oscillation frequency can decrease with temperature. For example, consider oscillator circuits which rely on repeated charging and discharging cycles of a capacitor to generate an oscillating voltage signal. A problem with such oscillator circuits can be that the rate of current flow on and off the capacitor  $C$  increases with increasing temperature. As a result, the capacitor charges and discharges faster at high temperatures and thus reaches respective upper and lower voltage limits in less time. This means that the frequency of the oscillating signal increases with temperature and hence such oscillators are unreliable in timing applications.

Embodiments of the present invention seek to provide oscillator circuits having improved temperature characteristics.

According to a first aspect of the present invention, there is provided oscillator circuitry comprising a capacitor; capacitor charging means arranged to supply a current to charge the capacitor to a first predetermined threshold voltage; capacitor discharging means arranged to discharge the capacitor to a second predetermined threshold voltage; and switching means arranged to switch between a capacitor discharging mode and a capacitor charging mode responsive to reaching at least one of said threshold voltages, wherein the at least one threshold voltage is determined by a threshold setting means which

**THIS PAGE BLANK (USPTO)**

provides a voltage threshold which varies to compensate for changes in temperature.

Preferably, the threshold setting means comprises a current source and a resistive means which varies in resistance in dependence upon temperature.

In preferred embodiments, the switching means comprises a comparator arranged to monitor voltage across the capacitor and to trigger a change between the discharging and charging modes.

In such case, the comparator is connected to a first control transistor which sets the first and second predetermined threshold voltages of the capacitor.

The first control transistor may be arranged to selectively bypass an element of a resistive chain.

Preferably, the comparator is also connected to a second control transistor which controls current flow to facilitate charging and discharging of the capacitor means.

Typically, the resistive means comprises one or more diode-connected transistors.

Each said capacitor charging means comprising a current source and preferably an IPTAT current source. Preferably, each said capacitor discharging means comprises a current source of the same type.

Embodiments of the present invention will now be described by way of example only with reference to the accompanying drawings in which:

**THIS PAGE BLANK (USPTO)**

Figure 1 shows a first embodiment of an oscillator circuit;

Figure 2 shows another oscillator circuit embodying the present invention; and

Figure 3 shows the variation of output voltage over time for the oscillator of Figure 2 at two different temperatures.

One type of oscillator circuit 10 is shown in Figure 1. The oscillator circuit 10 comprises a first power supply rail 12 and a second power supply rail 14. A first current source 16 is connected between the first power supply rail 12 and a first transistor M1 to generate IPTAT, a current proportional to absolute temperature. The transistor M1 has its controllable path connected between the first current source 16 and a second IPTAT current source 18 which is itself connected to the second power supply rail 14. The first current source 16, the transistor M1 and the second current source 18 are connected in series between the first power supply rail 12 and the second power supply rail 14.

A capacitor C has a first terminal connected to a node 20 between the first current source 16 and the transistor M1. The second terminal of the capacitor C is connected to the second power supply rail 14. A comparator 30 is disposed in the circuit 10 so as to comprise a switching device. The comparator 30 has a first (positive) input connected to the first terminal of the capacitor C and the node 20 between the first current source 16 and the transistor M1. A second (negative) input of the comparator 30 is connected to a node 32 of a resistive chain comprising first, second and third resistors  $R_1$ ,  $R_2$  and  $R_3$ . The resistors  $R_1$ ,  $R_2$  and  $R_3$  are connected in series between the first power supply rail 12 and the second power supply rail 14. The

**THIS PAGE BLANK (USPTO)**

node 32 to which the second input of the comparator 30 is connected is at the junction between the first resistor  $R_1$  and the second resistor  $R_2$  of the resistive chain  $R_1$ ,  $R_2$  and  $R_3$ .

The output 34 of the comparator 30 is supplied to the control terminal of a further transistor M2 which has its controllable path connected between the second power supply rail 14 and a node 36 between the second resistor  $R_2$  and the third resistor  $R_3$  of the resistive chain  $R_1$ ,  $R_2$  and  $R_3$ . The output 34 of the comparator 30 is also supplied to the control terminal of the first transistor M1. The first and second transistors M1 and M2 are thus both controlled by the output signal of the comparator 30.

In the above circuit there are two current sources 16,18. The first current source 16 produces the current  $I$  and the second current source 18 produces the current  $2I$ . In the charging phase of the capacitor, the transistors M1 and M2 are turned off. With the transistor M1 in an off state, the current  $I$  from the first current source 16 is supplied to the first terminal of the capacitor C. The voltage  $V_1$  on the capacitor C (i.e. the voltage on the first terminal of the capacitor referred to the second supply rail) rises until it reaches the voltage  $V_2$  of the junction between the first and second resistors  $R_1$  and  $R_2$  referred to the second supply rail 14.

When the voltage  $V_1$  on the capacitor C reaches the voltage  $V_2$  at the node 32, the transistors M1 and M2 are turned on. With the transistor M1 turned on, the capacitor C enters its discharging phase. The capacitor C is discharged by a predetermined amount. Since the conducting transistor M2 bypasses (shorts out) the third resistor  $R_3$ , the voltage  $V_2$  at the node 32 referred to the power supply rail 14 is reduced to a lower voltage. The

**THIS PAGE BLANK (USPTO)**

capacitor C discharges until a lower threshold is reached at which point in time the comparator switches back thereby turning off the transistors M1 and M2 to begin the charging cycle again.

Thus the capacitor C is charged by the first current source 16 until an upper threshold voltage close to the supply voltage is reached. The current supply to the capacitor is then "reversed", such that the capacitor C is discharged until a lower threshold voltage close to zero volts is reached. The current supply is "reversed" again and the cycle repeated. Repeat cycles of charging and discharging the capacitor C produce voltage oscillations on the capacitor referred to the second power supply rail 14. The voltage across the capacitor plates represents a substantially triangular waveform over time. A square wave for example for use in timing applications can be produced from the triangular wave by taking the output of an inverter having its input connected to the capacitor or the output of the comparator.

Figure 2 shows an oscillator circuit 100 in accordance with an embodiment of the invention which is capable of generating an output signal having a frequency which is substantially independent of temperature variations. The oscillator circuit 100 comprises a first power supply rail 112 and a second power supply rail 114. A first IPTAT current source 116 is connected between the first power supply rail 112 and a first transistor M3. The transistor M3 has its controllable path connected between the first current source 116 and a second IPTAT current source 118 which is itself connected to the second power supply rail 114. The first current source 116, the transistor M3 and the second current source 118 are connected in series between the first power supply rail 112 and the second power supply rail 114.

**THIS PAGE BLANK (USPTO)**

A capacitor  $C'$  has a first terminal connected to a node 120 between the first current source 116 and the transistor M3. A second terminal of the capacitor  $C'$  is connected to the second power supply rail 114. A comparator 130 is disposed in the circuit 100 so as to comprise a switching device. The comparator 130 has a first (positive) input connected to the first terminal of the capacitor  $C'$  and the node 120 at the junction between the first current source 116 and the transistor M3. A second (negative) input of the comparator 130 is connected to a node 132 of a component chain comprising in series a third IPTAT current source 150, a diode-connected transistor M5 and a resistor R. The third current source 150 is connected between the first power supply rail 112 and the diode-connected transistor M5. The resistor R is connected between the diode-connected transistor M5 and the second power supply rail 114. The node 132 to which the second input of the comparator 130 is connected is at the junction between the third current source 150 and the diode-connected transistor M5.

The output 134 of the comparator 130 is supplied to the control terminal of a transistor M4 which has its controllable path connected between the second power supply rail 114 and a node 136 at the junction between the diode-connected transistor M5 and the resistor R. The output 134 of the comparator 130 is also supplied to the control terminal of the first transistor M3. The first and second transistors M3 and M4 are controlled by the output signal 134 of the comparator as will be explained below.

In use, the capacitor  $C'$  is charged and discharged by the first and second current sources 116 and 118, respectively. The first current source 116 produces the current  $I$ . In the charging phase the transistors M3 and M4 are both turned off. With the

**THIS PAGE BLANK (USPTO)**

transistor M3 turned off, the current  $I$  from the first current source 116 is supplied to the first terminal of the capacitor  $C'$ . As the charge on the plate of the capacitor  $C'$  accumulates, the voltage  $V_3$  across the capacitor increases until it reaches the voltage  $V_4$  between the junction 132 and the second power supply rail 114. With the transistor M4 turned off the voltage  $V_4$  depends on the resistance of the circuit branch containing the diode-connected transistor M5 and the resistor  $R$ . That is, in the charging phase the upper voltage threshold of the capacitor is determined by the voltage across the series combination of the diode-connected transistor M5 and the resistor  $R$ .

When the voltage  $V_3$  across the capacitor  $C'$  reaches that between the node 132 and the second power supply rail 114, the output of the comparator 130 changes state. The change in the state of the output of the comparator 130 is effective to switch the transistors M3 and M4 on. When the transistor M3 is turned on the capacitor  $C'$  enters its discharging phase. The capacitor  $C'$  is discharged by a predetermined amount. For example, the second current source 118 passes a current  $2I$  and the first current source passes a current  $I$ , the capacitor is discharged by an amount  $I$  (where  $I=2I-I$ ). That is, the voltage  $V_3$  across the plates capacitor  $C'$  is reduced to a lower threshold voltage determined by the voltage  $V_4$  at node 132 referred to the second power supply rail 114. The voltage  $V_4$  at the node 132 is dependent only upon the resistance of the diode-connected transistor M5 since the transistor M4 is now turned on and defines a lower resistance pathway between the second power supply rail 114 and the diode-connected transistor M5.

When the capacitor  $C'$  is discharged to the extent that this lower voltage threshold is reached the output of the comparator changes state again and the transistors M3 and M4 are switched

**THIS PAGE BLANK (USPTO)**

back to their off states to begin the charging cycle again. The above described charging and discharging phases are repeated many times to generate an oscillating triangular waveform. The oscillating triangular waveform is converted to a square waveform by taking the output of an inverter having its input connected to the capacitor.

Figure 3 illustrates how the capacitor voltage generated by the embodiment of Figure 2 varies with time at two different temperatures. Voltage increases along the y-axis and the time along the X-axis. The solid triangular wave 302 represents the voltage  $V_3$  across the capacitor plates at a first temperature  $T_1$ . The broken triangular waveform 304 represents the voltage  $V_3$  across the capacitor plates at a temperature  $T_2$  which is higher than the first temperature  $T_1$ . (i.e.  $T_2 > T_1$ ).

At the lower temperature  $T_1$ , the voltage  $V_3$  across the plates of the capacitor  $C'$  oscillates between an upper limit  $UL$  and a lower limit  $LL_{T_1}$ . The upper  $UL$  is defined during the charging phases of the capacitor  $C$  by the voltage across the series combination of the diode-connected transistor  $M_5$  and the resistor  $R$ . The lower limit  $LL_{T_1}$  is defined during the discharging phases of the capacitor  $C'$  by the voltage across the diode-connected transistor  $M_5$  only. The result of continuous oscillation between these upper and lower limits  $UL$ ,  $LL_{T_1}$  is a substantially triangular waveform having a trough-to-trough period of  $t_1$  and thus a frequency of  $1/t_1$ .

At the higher temperature  $T_2$  the voltage on the capacitor  $C'$  oscillates between the same upper limit  $UL$  and a lower limit  $LL_{T_2}$ . The upper limit  $UL$  is defined in the charging phase of the capacitor  $C'$  in the same way as above. As temperature increases the charging and discharging currents increase and hence the

**THIS PAGE BLANK (USPTO)**

capacitor charges and discharges to its upper and lower threshold voltages at a greater rate. This is demonstrated by the steeper gradients of the waveform designated by reference numeral 304 compared with the gradients of the waveform 302 on Figure 3. The lower voltage threshold during the discharging phase of a capacitor  $C'$  in a circuit such as that shown in Figure 2 is dependent on the resistance of the diode-connected transistor. The lower voltage threshold  $LL_{T_2}$  at temperature  $T_2$  is less than the lower voltage threshold  $LL_{T_1}$  at the temperature  $T_1$ . The voltage across the diode-connected transistor M5 gets smaller with increasing temperature and hence the lower voltage threshold  $LL_{T_2}$  at higher temperatures is shifted to a lower value by a potential difference  $\Delta V$ . The downward shift in the lower voltage threshold means that the capacitor  $C'$  must undertake a larger voltage swing between the upper and lower voltage thresholds defining the charged and discharged states. The larger voltage swing compensates for the increased charging and discharging rates such that the period of oscillation at the higher temperature is substantially the same as in the lower temperature case (i.e. the period  $t_1$  = the period  $t_2$ ). That is, the oscillation frequency remains the same at the higher temperature  $T_2$  as it is at the lower temperature  $T_1$ .

Oscillator circuits embodying the present invention can provide an oscillating waveform at frequencies which do not vary in dependence upon temperature conditions. This is achieved by employing threshold voltage setting means which can vary a voltage level at which the oscillator switches between oscillation cycles in dependence upon the temperature of the environment in which the oscillator is operating.

In the preferred embodiment a current source is implemented as a single diode-connected transistor M5. The skilled person would

THIS PAGE BLANK (USE)

appreciate that while only one such diode-connected transistor is designated by reference numeral M5 two or more diode-connected transistors may be coupled together and used to facilitate larger voltage swings.

Embodiments of the present invention are not limited to the configuration of the embodiment described herein. Specifically the embodiment described herein is intended to illustrate one example of a configuration which may be used to implement the invention.

**THIS PAGE BLANK (USPTO)**

## CLAIMS:

## 1. Oscillator circuitry comprising:

a capacitor;

capacitor charging means arranged to supply a current to charge the capacitor to a first predetermined threshold voltage;

capacitor discharging means arranged to discharge the capacitor to a second predetermined threshold voltage; and

switching means arranged to switch between a capacitor discharging mode and a capacitor charging mode responsive to reaching at least one of said threshold voltages, wherein the at least one threshold voltage is determined by a threshold setting means which provides a voltage threshold which varies to compensate for changes in temperature.

2. Circuitry as claimed in claim 1, wherein the threshold setting means comprises a current source and a resistive means which varies in resistance in dependence upon temperature.

3. Circuitry as claimed in claim 1 or 2, wherein the switching means comprises a comparator arranged to monitor voltage across the capacitor and to trigger a change between the discharging and charging modes.

4. Circuitry as claimed in claim 3, wherein the comparator is connected to a first control transistor which sets the first and second predetermined threshold voltages of the capacitor.

5. Circuitry as claimed in claim 4, wherein the first control transistor is arranged to selectively by-pass an element of a resistive chain.

**THIS PAGE BLANK (USPTO)**

6. Circuitry as claimed in any of claims 3 to 5, wherein the comparator is connected to a second control transistor which controls current flow to facilitate charging and discharging of the capacitor means.

7. Circuitry as claimed in any of claims 2 to 6, wherein the resistive means comprises one or more diode-connected transistors.

8. Circuitry as claimed in any preceding claim, wherein the capacitor charging means comprises a current source.

9. Circuitry as claimed in any preceding claim, wherein the capacitor discharging means comprises a current source.

10. Oscillator circuitry substantially as described herein with reference to Figure 2 of the accompanying drawings.

**THIS PAGE BLANK (USPTO)**

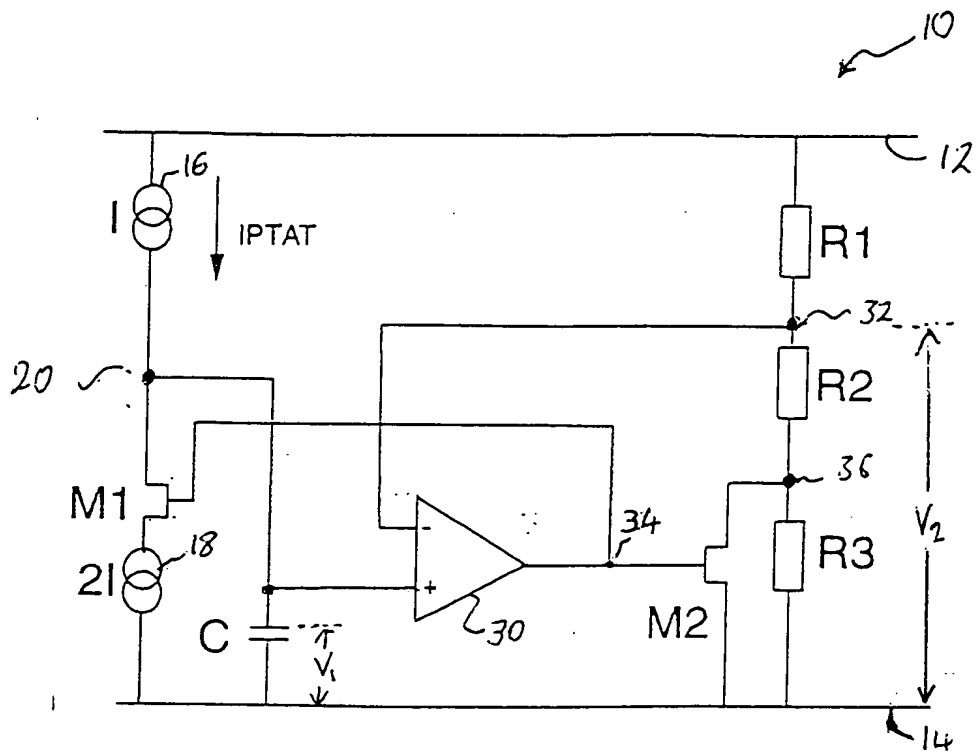


FIG. 1

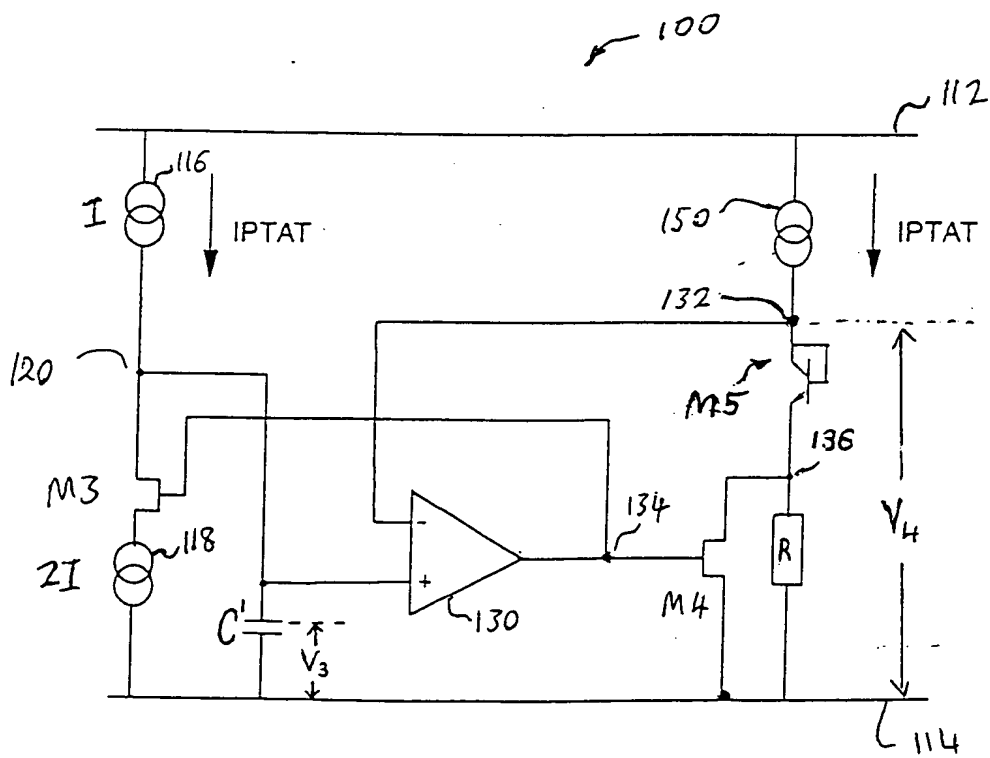


FIG. 2

**THIS PAGE BLANK (USPTO)**

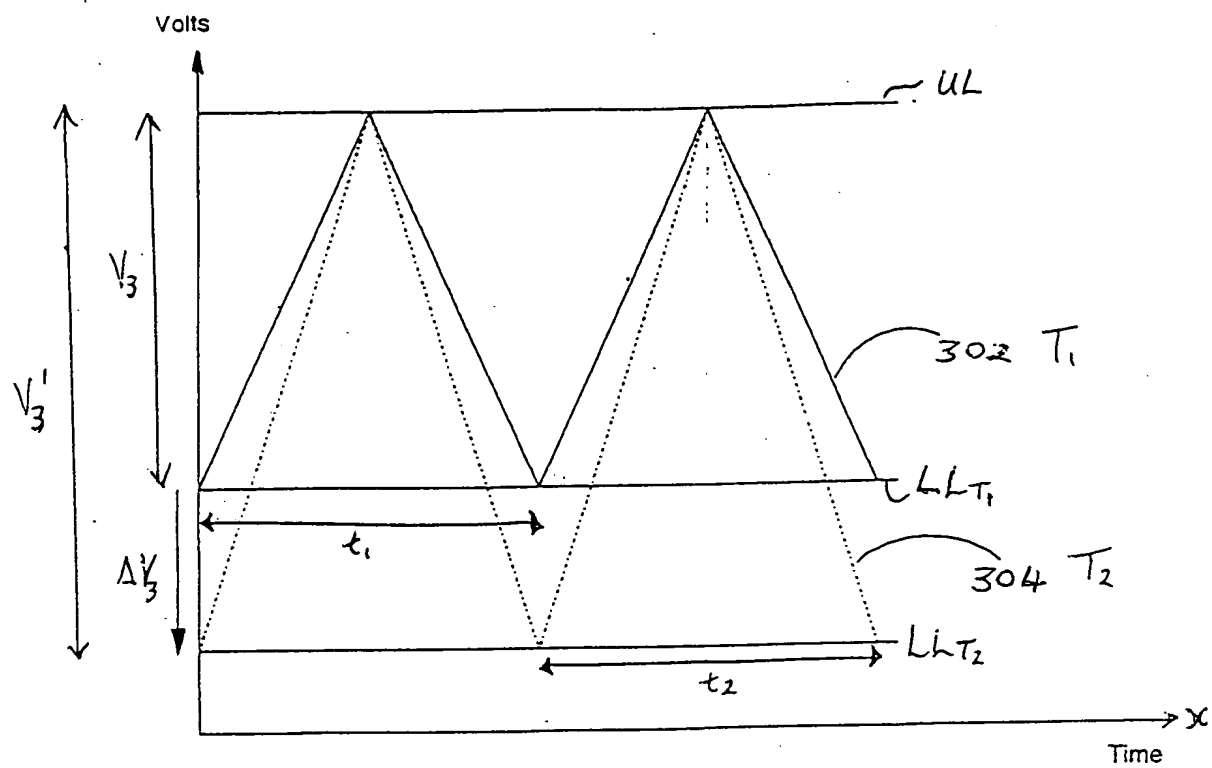


FIG. 3

**THIS PAGE BLANK (USPTO)**